Precision Improvement of Power-Efficient Capacitive Senor Readout Circuit Using Multi-Nested Clocks

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***Abstract*—This paper proposes a clock strategy to improve the precision of power-efficient readout circuit for capacitive sensor. To achieve high power efficiency, capacitive sensor such as MEMS accelerometer is designed with open-loop architecture rather than close-loop one. In the open-loop architecture, the capacitance variation of sensing element is limited to femto-farad level in order to overcome nonlinearity problem. However, due to this limitation, the signal charge from sensing element is weak and the interference charge due to coupling capacitance between clock wires and sensing electrodes becomes a significant issue. Therefore, split clock bus is employed to meet this challenge, but the split clock bus introduces the timing mismatch problem which causes charge injection sensitive to fabrication process and circuit operating voltage. As a result, the offset variation and nonlinearity of readout circuit will increase, and this will lead to reduction of precision. In this work, a clock scheme named "multi-nested clocks" is proposed to address the charge injection problem due to timing mismatch. The multi-nested clocks are demonstrated in a readout circuit fabricated using a 0.18-µm BCD process. The measurement results show that compared to the readout circuit using traditional clock, the readout circuit using the multi-nested clocks reduces the equivalent input offset from 1.66fF to 0.25fF, the offset variation from 1.4fF to 0.2fF and the nonlinearity from 5.5% to 0.9%.**

***Index Terms*—Capacitive sensor, MEMS, readout circuit, sensor interface, charge injection, high precision, nonlinearity, multi-nested clocks.**

I. Introduction

MEMS (Micro-electromechanical Systems) capacitive sensor, especially accelerometer, is one of the most important large-scale medical data collectors in disease research such as cardiovascular diseases, diabetes and psychosis [1]-[3]. It plays an important role in continuous physical activity monitoring and health care applications [4][5]. In these applications, the sensors are powered by battery, thus high energy efficiency is required to extend battery life. As a result, the MEMS accelerometers for wearable monitoring devices are designed with open-loop architecture rather than close-loop one to achieve low power consumption [6]. In the open-loop architecture, the nonlinearity of the mechanical sensing element significantly increases with the increase of the capacitance variation of the sensing element. Therefore, the capacitance variation needs to be limited to femto-farad level to suppress the nonlinearity to an acceptable level. However, the fact that the femto-farad level capacitance variation of sensing element is much lower than parasitic capacitance of sensing electrodes which is at pico-farad-level results in significant deterioration of gain error [7]. The gain error deterioration can be alleviated by the "Oversampling Successive Approximation (OSA) Readout technique" [7][8].

Compared to traditional readout circuit [9]-[12], the OSA based readout circuit shows advantages in gain accuracy and power efficiency. However, the OSA based readout circuit is sensitive to interference charge due to the coupling capacitance between clock wires and sensing electrodes, which introduces such a significant offset that it can easily overwhelm the signal amd saturate the readout circuit. Traditionally, the correlated double sampling (CDS) technique is employed to cancel the offset of capacitive readout circuit introduced by amplifier [11]-[13]. But the offset introduced by the interference charge from clock wires can hardly be sampled and cancelled with the CDS technique, as it's difficult to predicate which clock wire the interference charge will come from and when the interference charge will come. To avoid this unpredictable interference charge from clock wires, this work employs a layout-level solution named "split clock bus", in which the clock wires are symmetrically routed outside circuit blocks rather than inside circuit blocks to eliminate coupling effect in the physical layout. Although the high precision auto-calibration technique can be employed to reduce the offset of readout circuit resulted from interference charge to sub-fF level [14]-[16], the split clock bus can reduce the offset without additional redundancy calibration circuit. However, this split clock bus has a drawback that it causes "timing mismatch" which introduces charge injection varying with fabrication

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process. This variable charge injection will result in offset variation and nonlinearity in the readout circuit. In this paper, a clock scheme named "multi-nested clocks" is proposed to solve this problem. Compared with the traditional charge injection reduction methods such as the dummy switch [17][18], the injection-nulling switch [19], the low swing driver [20] and the multi-frequency operation [21], the proposed method can not only reduce the charge injection, but also reduce the charge injection variation, thus improve the precision of readout circuit.

The rest of the paper is organized as follows. In Section II, the phenomenon of timing mismatch is illustrated in detail. In Section III, charge injection of readout circuit are analyzed with four models. Multi-nested clocks for minimizing the charge injection and charge injection variation of each model are described. In Section IV, the multi-nested clocks are demonstrated in the OSA based readout circuit and the measurement results are presented. The conclusions are then drawn in Section V.

II. Timing Mismatch

A. Split clock wire and timing mismatch

The readout circuit based on the OSA technique shown in Fig. 1 is composed of the common-mode charge controller (CMC) to absorb the unwanted common-mode charge produced by the sensor and the capacitance-to-voltage convertor (CVC) to convert the capacitance difference ($C_{S1} - C_{S2}$) of the sensing element to the differential output voltage ($V_{O+} - V_{O-}$). The capacitors C_{P1} and C_{P2} represent the parasitic capacitance between the sensing electrodes (IN+ and IN-) and the ground. The capacitors C_{P3} and C_{P4} represent the coupling capacitance between the sensing electrodes and the interference voltage source V_{INT}. The capacitor C_L and the switches in the small dash box represent the switched-capacitor loads such as the switched-capacitor common-mode feedback network (SC-CMFB) used in the readout circuit [22]. The ideal output of the readout circuit is in proportion to the sensing element's capacitance difference,

$$V_O = V_{O+} - V_{O-} = \frac{V_R}{C_i}(C_{S1} - C_{S2}) \quad (1)$$

where V_R is the reference voltage, C_i is the integration capacitor. In this paper, only the charge injection related issues resulted from timing mismatch are discussed, as other properties of this readout circuit were explained in [7].

The most interference charge occurs in the sensing electrodes IN+ and IN- due to the coupling capacitances C_{P3} and C_{P4}. Taking these coupling capacitances into consideration, the equation (1) becomes,

$$V_O = \frac{V_R}{C_i}(C_{S1} - C_{S2}) + \frac{V_{INT}}{C_i}(C_{P3} - C_{P4}) \quad (2)$$

According to the typical 3-axis MEMS accelerometer from STMicroeletronics [23][24], the typical variation of the sensing element's capacitance difference ($C_{S1} - C_{S2}$) is 1fF when 1g acceleration is applied. The reference voltage V_R is 0.9V. The

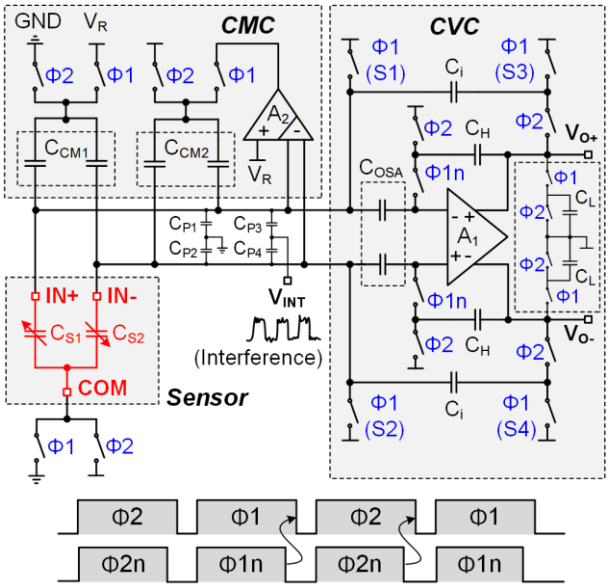


Fig. 1. Readout circuit based on the OSA technique.

interference source V_{INT} usually stems from the clock wires and it is at a similar voltage level to VDD (1.8V). As a result, if the mismatch of the coupling capacitances C_{P3} and C_{P4} reaches 0.5fF, the interference charge would be large enough to overwhelm the signal charge.

Practically, it is difficult to match the coupling capacitances in physical layout in CMOS process to a sub-fF level. Thus, the interference charge is inevitable and it is undeterminable as well. Although calibration method can be employed to reduce the mismatch, additional design will be needed and the noise from V_{INT} is still inevitable. A better way to deal with the interference charge caused by the coupling capacitances C_{P3} and C_{P4} is use of the "split clock bus" rather than the "concentrated clock bus" in the physical layout, as shown in Fig. 2. With the split clock bus, all the clock wires are routed outside the circuit blocks to avoid any undesirable coupling with the sensing electrodes. The clock wire is "split" because the circuit structure is fully differential. For example, the bus-1A drives the switches in one differential circuit branch (the switches S1 and S3 in Fig. 2(b)), and the bus-1B drives the switches in the other differential circuit branch (the switches S2 and S4 in Fig. 2(b)). In this way, the clock wires will not have undesirable coupling with the wires inside the blocks.

However, the split clock bus causes a new problem "timing mismatch" which includes delay mismatch and slew-rate mismatch, as shown in Fig. 3. This is because the two branches of the split bus (e.g., bus-1A and bus-1B in Fig. 2(b)) are on two different physical routes from which any mismatch of coupling capacitances to the nearby ground/power/clock wires will lead to the timing mismatch between clocks the driving two differential circuit branches. This timing mismatch then introduces the charge injection which varies with fabrication process and is therefore difficult for traditional charge injection reduction methods to deal with.

B. Charge injection models of timing mismatch

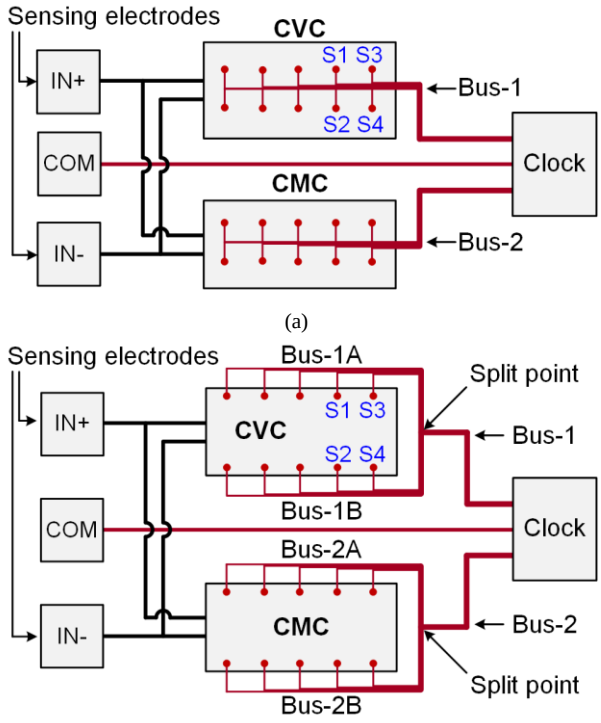


Fig. 2. Layout consideration of clock routing for the readout circuit. (a) Concentrated clock bus. (b) Split clock bus.

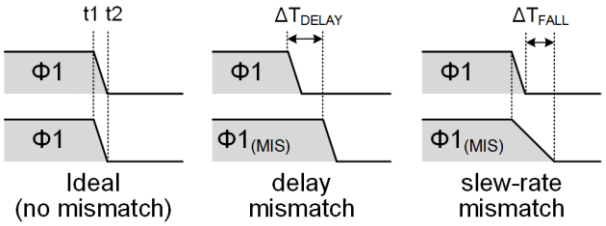


Fig. 3. Timing mismatch between the clocks driving two differential branches in the split clock bus.

The charge injections resulted from the timing mismatch can be modelled as follows. There are four types of charge injection models as shown in Fig. 4, which are derived from the schematic in Fig. 1(a) with the consideration of the charge injections to all the capacitors. Although these models are derived from the OSA based readout circuit, they are also effective to predicate the charge injections in the conventional switched-capacitor readout circuit.

The Type-I model shown in Fig. 4(a) is the classical charge injection model which consists of one switch and one capacitor [17][18]. This model is only suitable for parasitic capacitance, such as the capacitors C_{P1} and C_{P2} in Fig. 1, one of whose terminals is permanently connected to DC sources. The Type-II model shown in Fig. 4(b) is suitable to describe the charge injection to those capacitors, both of whose terminals are connected to switches, such as the capacitor C_i. The Type-III model shown in Fig. 4(c) is used to describe the charge injection to the two capacitors in different circuit branches but with a common node, such as the capacitors C_{S1} and C_{S2}. The capacitors C_{S1} and C_{S2} are also known as "capacitive half-bridge" [25]. The Type-IV model shown in Fig. 4(d)

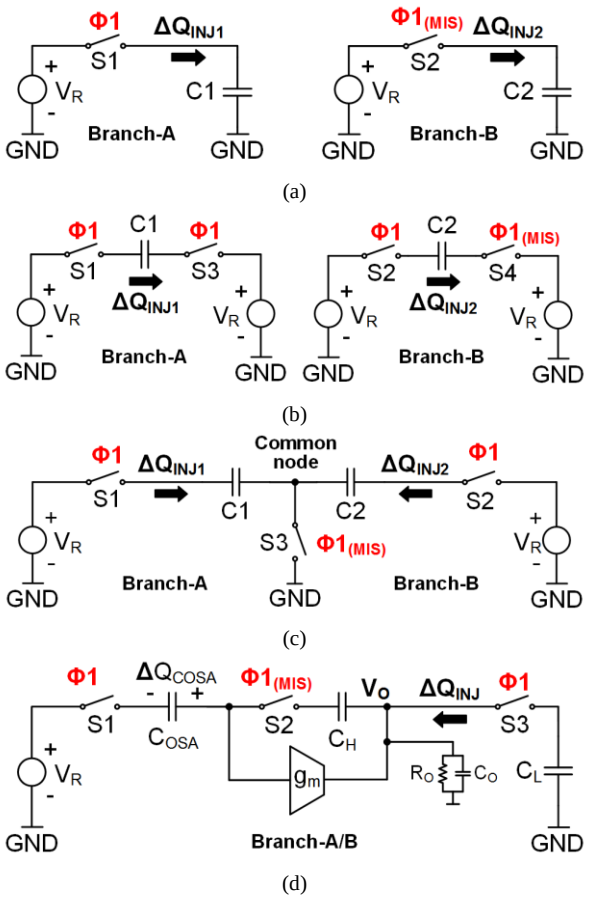


Fig. 4. Charge injection models. (a) Type-I model for injections to parasitic capacitors (e.g., C_P). (b) Type-II model for injections to operational capacitors (e.g., C_i). (c) Type-III model for injections to capacitive half-bridge (e.g., C_{S1}&C_{S2}, C_{CM1} and C_{CM2}). (d) Type-IV model for kickback charge injections to capacitors in the feedback network (e.g., C_H and C_{OSA}).

describes the kickback charge injection to the capacitors in the feedback network, such as the capacitors C_H and C_{OSA}. This type of charge injection is a result of voltage spike of the output terminals [26].

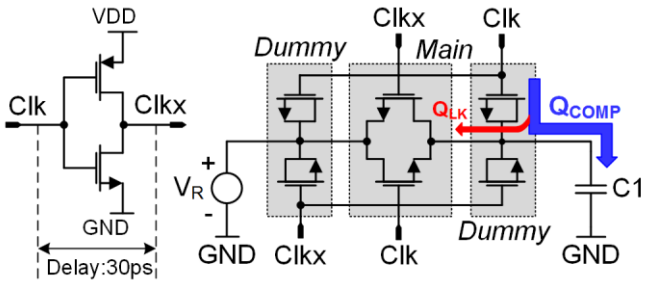
These models are analyzed only in the phase Φ1. This is because the readout circuit's output is affected by the charge injection only generated in the phase Φ1.

III. Reduction of Variation of Charge Injection

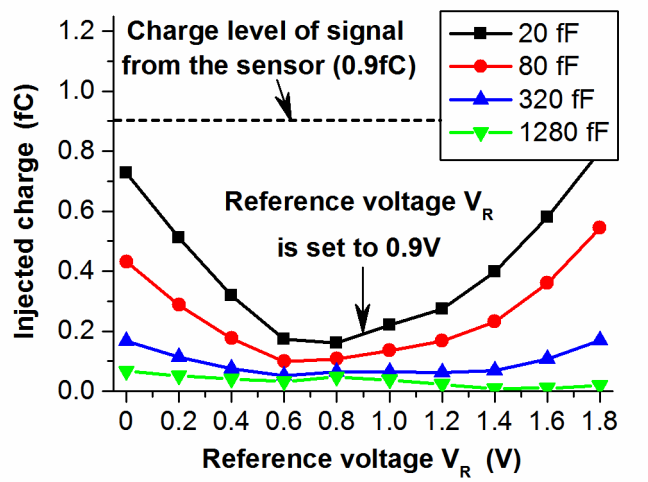
A. *Analysis of Type-I model*

Traditionally, the reduction of the charge injection in Type-I model can be achieved by using the dummy switches [18], as shown in Fig. 5(a). Ideally, the amount of the charge compensated by the dummy switches is the same as the amount of the charge injected by the main switch, therefore completely compensating the charge injection. However, this method will lose its effectiveness if any of the following three parameters varies: the reference voltage V_R (it is used as bias voltage), the load capacitor C1 and the slew-rate of the clock. This is explained as follows and the solutions are given thereafter.

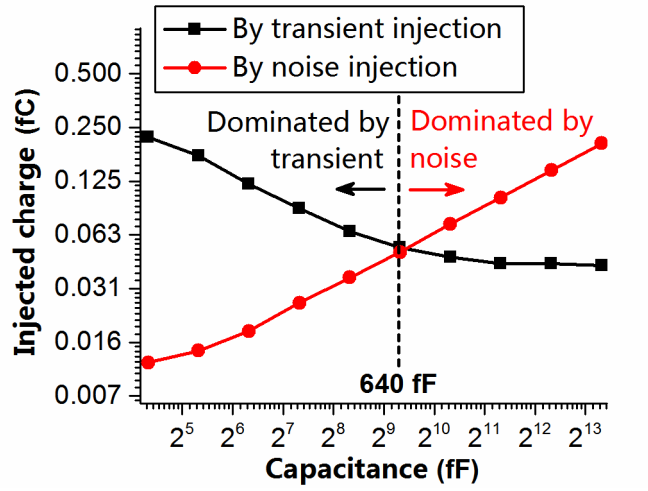
When biased with different voltages, the main switch will inject different amount of charge [17]. The value of injected charge is the smallest when the bias voltage is near half of the power supply voltage (i.e., 0.8V-1.0V). This is because the



(a)



(b)



(c)

Fig. 5. Basic charge injection properties of the traditional switch. (a) Schematic of the traditional switch configured as Type-I model. (b) Injected charge versus bias voltage V_R. (c) Injected charge versus capacitance of C1.

charge injections from P-type MOSFET and N-type MOSFET of the main switch cancel each other well when the main switch is biased in such a way. Therefore, all the reference voltages in the readout circuit are set to be 0.9 V to minimize charge injection, as shown in Fig. 5(b).

The capacitance of C1 affects amount of the injected charge from the traditional switch to the capacitor C1 in two aspects: the transient charge injection due to clock activities and the thermal noise charge injection due to on-resistance of transistor. The smaller the capacitance of C1 is, the larger the transient charge injection will be. In Fig. 5(a), the falling-edge of the clock Clk is 30ps earlier than that of the inverse clock Clkx. Thus, the compensation charge Q_{COMP} from the dummy switches is injected before the main switch is completely shut down. As a result, part of the compensation charge Q_{COMP} is leaked via the main switch and the compensation is less effective. Amount of the leaked compensation charge Q_{LK} is adversely proportional to the value of C1. Thus, small value of C1 will lead to ineffective compensation and high transient charge injection. On the other hand, the larger the capacitance of C1 is, the larger the thermal noise charge injection will be. According to equipartition theorem, the thermal noise charge from the transistors sampled by the capacitor C1 increases with the increase of the capacitance value of C1 [27].

The transistor-level simulation of the Type-I model is shown in Fig. 5(c). The channel widths/lengths of P-type MOSFET in the main switch, P-type MOSFET in the dummy switches, N-type MOSFET in the main switch and N-type MOSFET in the dummy switches are 2μm/200nm, 1μm/200nm, 1μm/200nm and 500nm/200nm, respectively. These dimensions are also used in the remaining part of this paper. It is clear from Fig. 5(c) that for the capacitor C1 with a large capacitance (significantly larger than 640fF), it is essential to reduce the thermal noise charge injection as the overall injected charge is dominated by the thermal noise charge injection. For C1 with a small capacitance (significantly less than 640fF), it is important to reduce the transient charge injection as the overall injected charge is dominated by the transient charge injection. This work focuses on reducing the transient charge injection, as the sensing element capacitance is typically smaller than 640fF and the thermal noise charge injection is not dominant.

The mismatch variation of the slew-rate or slope of the clock Clk makes the charge injection of traditional switch variable. This was explained in detail in [17]. In this paper, a switch named as "local slew-rate controlling (LSC) switch" shown in Fig. 6(a) is employed to reduce the variation of the charge injection. As can be seen in the figure, an inverter chain composed of N inverters is added to the traditional switch to reduce the effect of slew-rate mismatch on charge injection. The transistor-level simulation results in Fig. 6(b) show that with the traditional switch, the amount of injected charge varies significantly with change of the slew-rate mismatch. However, with the LSC switch, the variation of charge injection is significantly reduced. With N=2 and 4, the variation is reduced from 336% per decade to 87.5% per decade and 5% per decade, respectively. It is unnecessary to make N larger than 4, as the variation is already negligible (5% per decade) when N=4 and the additional delay due to large N can be detrimental to the reduction of the delay mismatch which is to be explained in the next section.

In summary, the techniques to deal with charge injection and charge injection variation are as follows. Firstly, reference voltage is set to be 0.9V for the least charge injection. Secondly, LSC switch is used to reduce the variation of charge injection, which is caused by variation of slew-rate mismatch. It is worth noting that although these techniques are derived from Type-I model, they are also applicable to the other three models.

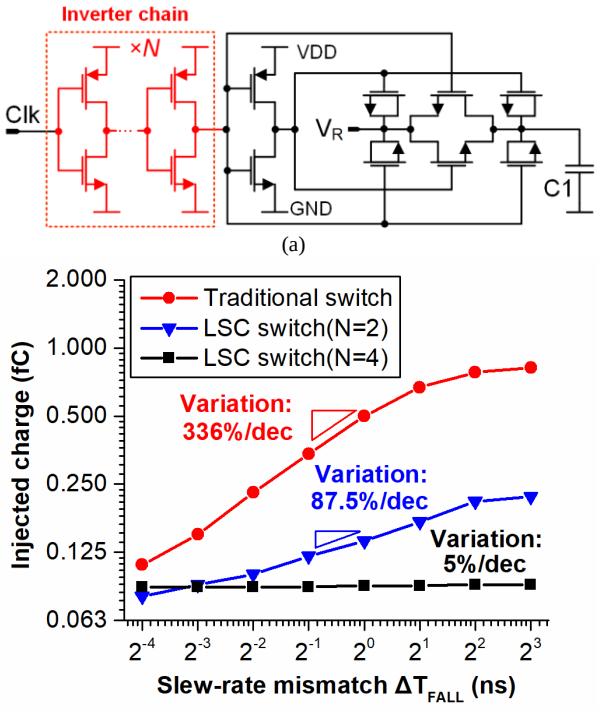


Fig. 6. Charge injection properties of LSC switch. (a) Schematic of LSC switch configured as Type-I model. (b) Charge injection with different slew-rate mismatch. The value of the capacitor C1 is 100fF.

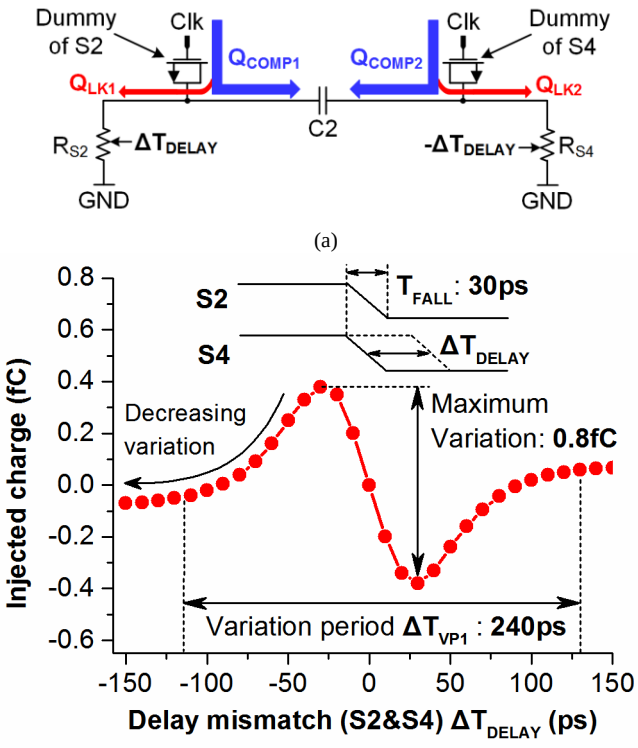


Fig. 7. Charge injection properties of Type-II model. (a) Equivalent circuit of Type-II model. (b) Transistor-level simulation results.

B. *Analysis of Type-II model*

Delay mismatch is the main consideration of Type-II model shown in Fig. 4(b) as the slew-rate mismatch can be solved by employing the LSC switches. The charge injection of the model is explained by the equivalent circuit in Fig. 7(a). The switches S2 and S4 are modeled as the variable resistors R_{S2} and R_{S4}, respectively. The resistance of theses variable resistors varies with the delay mismatch ΔT_{DELAY}. If $\Delta T_{DELAY} = 0$, the switches S2 and S4 shut down simultaneously and R_{S2} is equal to R_{S4}. As a result, the injected compensation charges Q_{COMP1} from S2 and Q_{COMP2} from S4 are equal and the total charge injected to C2 is zero. If $\Delta T_{DELAY} > 0$, the switch S2 shuts down earlier than the switch S4 does and the resistance of R_{S2} is larger than that of R_{S4}. Thus, the charge Q_{COMP2} from S4 is leaked (Q_{LK2}) and the charge injected to C2 is not zero and it is dominated by the charge Q_{COMP1}. If $\Delta T_{DELAY} < 0$, the charge injected to C2 is not zero either and it is dominated by Q_{COMP2}.

The transistor-level simulation results in Fig. 7(b) show that the maximum variation of the charge injection caused by the delay mismatch can reach 0.8fC, i.e., 89% of the signal charge (0.9fC) in Fig. 5(b). The variation of charge injection decreases if the variation of delay mismatch ΔT_{DELAY} is not in the range of ΔT_{VP1} whose value is about 8 times of the falling time T_{FALL} of clocks. Thus, if the two clocks with a delay offset ΔT_{OFFSET} larger than ΔT_{VP1} (such as the clocks Φ1 and Φ1n shown in Fig. 8) are used to drive S2 and S4, the charge injection variation problem in Type-II model can be minimized.

C. *Analysis of Type-III model*

The major consideration of Type-III model shown in Fig. 4(c) is the delay of the switch S3. If S3 switches off earlier than the switches S1 and S2 do, the common node of the capacitors C1 and C2 floats, as shown on the left in Fig. 9(a). So any charge injected to C1 will also be injected to C2 via the floating common node, but in opposite direction. Thus, the charge Q_{INJ} injected from the switches S1 and S2 to the capacitors C1 and C2 is always differential charge injection.

If S3 switches off later than the switches S1 and S2 do, the common node of the capacitors C1 and C2 is grounded via R_{S3}, as shown on the right in Fig. 9(a). The resistor R_{S3} is the turn-on resistance of the switch S3. In this mode, the charge injected from the switch S1 flows to the ground GND via R_{S3} rather than flowing into C2, so does the charge injected from the switch S2. As a result, the charges (Q_{INJ1} and Q_{INJ2}) injected to the capacitors C1 and C2 are in the same direction and they are common-mode charge injection.

The above analysis indicates that by delaying the switch-off time of the switch S3, it can prevent injecting differential charge to the capacitors C1 and C2, therefore minimizing differential charge injection in Type-III model. As shown in the transistor-level simulation results in Fig. 9(b), when S3 switches off 10ns later than S1 and S2 do, the differential charge injected to the capacitors C1 and C2 (ΔQ1) is reduced by 18 times compared to the differential charge ΔQ2 where S3 switches off 10ns earlier than S1 and S2 do.

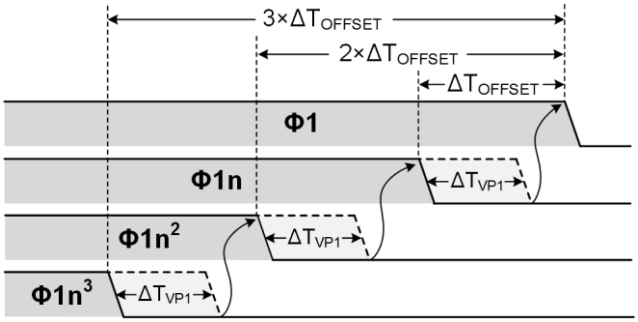
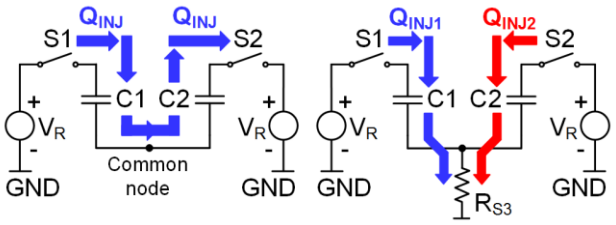
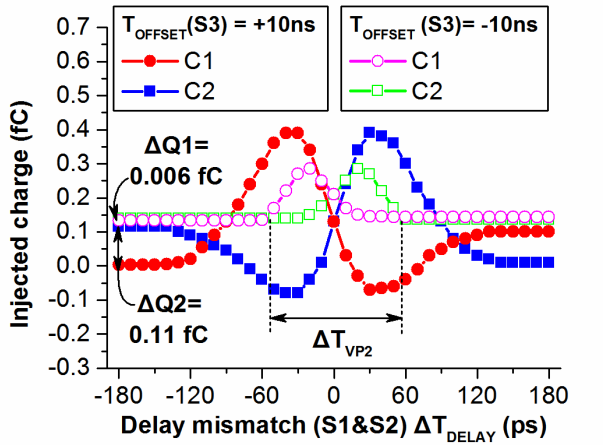


Fig. 8. Clock arrangement for reducing the variation of charge injection.



(a)



(b)

Fig. 9. Charge injection properties of Type-III model. (a) Equivalent circuit of Type-III model with different switch-off timing of S3. (b) Transistor-level simulation results on the effect of switch-off timing of S3.

It is worth noting that the variation of delay mismatch between clocks driving S1 and S2 also introduces variable differential charge injection while the variation is in the range of ΔT_{VP2} (similar to ΔT_{VP1} in Type-II model in Fig. 7(b)), as shown in Fig. 9(b). This is because the resistance of R_{S3} is not infinitesimal and very small coupling effect still exists. The solution is similar to that in Type-II model, i.e., the time offset ΔT_{OFFSET} between the clocks driving S1 and S2 is set to a value larger than ΔT_{VP2} in order to minimize the variation of charge injection.

Based on the above analysis, a clock scheme for practical capacitive half-bridges is proposed as shown in Fig. 10. In the scheme, three multi-nested clocks are needed to minimize the variation of charge injection, which turn off switches in the following sequence. The switches connected to the differential node A are turned off by the clock Φ1n^2 first, and then the switches connected to the differential node B are turned off by the clock Φ1n, finally the switches connected to the common node are turned off by the clock Φ1.

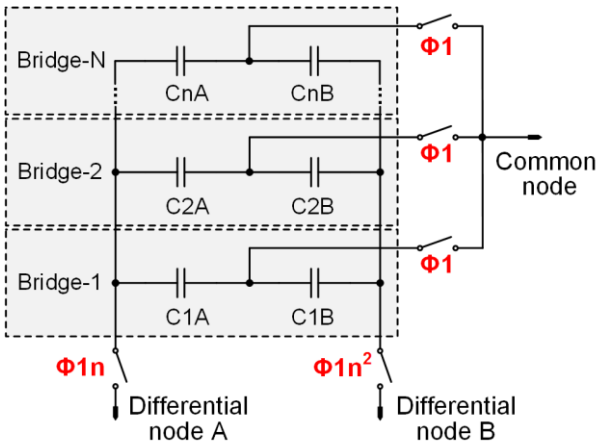


Fig. 10. Clock strategy to minimize the differential charge injection for multi-capacitive-bridge.

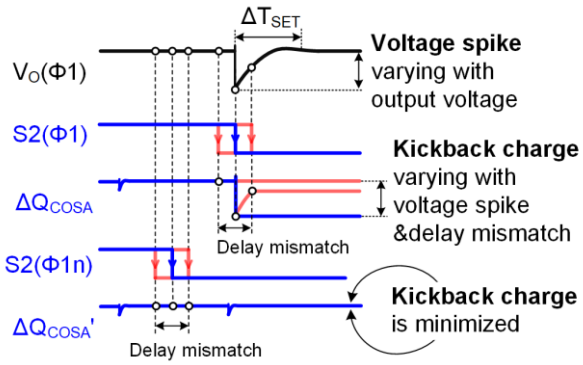


Fig. 11. Clock strategy to eliminate the kickback charge injection for capacitors in the feedback network.

D. Analysis of Type-IV model

The main consideration of Type-IV model shown in Fig. 4(d) is the kickback charge injection introduced by output voltage spike. It is well known that kickback noise in ADC is caused by the high-speed turnover of the regeneration comparator's output and it introduces reference source noise, code transition error and settling time degradation of amplifiers [26]. Similarly, in this work, the "kickback charge injection" is caused by the voltage spike of the readout circuit's output and it introduces both nonlinearity and input offset variation. The process of injection of kickback charge is described as follows.

Firstly, the voltage spike is caused by the charge injected from the switches connected to the output terminals, e.g., the switch S3 driven by phase Φ1 in Fig. 4(d). The voltage spike takes a time period ΔT_{SET} to settle, as shown in Fig.11. ΔT_{SET} depends on the gain-bandwidth product (g_m/C_0) of the amplifier. Then, as the switch S2 driven by the same phase Φ1 in Fig. 4(d) will turned off within the period ΔT_{SET} due to delay mismatch, the voltage spike injects an error charge ΔQ_{COSA} to the capacitor C_{OSA}. Finally, the error charge ΔQ_{COSA} is transferred to the integration capacitor C_i in the phase Φ2 (Fig. 1), producing output error.

Based on the above analysis, the output error due to kick back charge from the switch S3 varies with the change of delay mismatch between the switch S2 and the switch S3. This results in variation of input offset. Besides, the amount of kick back charge injected from the switch S3 varies with its bias voltage

which is equal to the output voltage V_O. This results in nonlinear output error. Thus the kick back charge injection introduces both nonlinearity and input offset variation.

The kickback charge injection can be minimized by driving the switch S2 with an earlier clock (Φ1n) than that driving the switch S3 (Φ1) in order to minimize the variation of kickback charge ΔQ_{COSA}, as shown in Fig. 11.

IV. Physical Verification

To apply the multi-nested clocks, the OSA readout circuit from [7] is decomposed into the four types of models described in Section III, as shown in Fig. 12. All the switches used in the readout circuit are the LSC switches. The timing diagram of the clocks is shown in Fig. 8 with ΔT_{OFFSET} being 10ns. The operational frequency is 100 kHz.

The OSA readout circuit from [7] is reproduced without changing circuit structure and the proposed multi-nested clocks are demonstrated in the reproduced circuit. The test configuration is shown in Fig. 13. Both the multi-nested clocks and the traditional clocks are generated on chip. Compared with the traditional clock generator, the chip area and the current supply of the multi-nested clock generator are increased by 125% (from 2,000μm^2 to 4,500μm^2) and 113% (from 80nA to 170nA at 100 kHz operation frequency), respectively. However, the additional area and power consumption introduced by the multi-nested clock generator are negligible in terms of the overall chip area and power consumption. A multiplexer controlled by off-chip signal is used to select clock. An on-chip test module is added to mimic the input signal charge of a sensor. The module is composed of the capacitors C_T and relevant switches. The capacitance of C_T is 20fF, which means that with an input test voltage V_T of 45mV, it can mimic 0.9fC input signal charge which is equal to the amount of signal charge produced by a sensing element's capacitance difference of 1.0fF. The readout circuit is fabricated with a commercial 1.8V 0.18μm BCD process. The photograph of the chip is shown in Fig. 14.

The test results of the readout circuit are shown in Fig. 15. The main experimental parameters are listed in Table I. The number of testing samples of the chip is 15. For the OSA readout circuit without the multi-nested clocks, the average equivalent input offset of the readout circuit is OS1=1.66fF. The offset variation is $\delta 1$=1.4fF (from 0.9fF to 2.3fF). The large offset variation indicates that the readout circuit is sensitive to the variation of fabrication process and this is due to the charge injection variation caused by the timing mismatch discussed in Section III. For the OSA readout circuit with the multi-nested clocks, the average equivalent input offset of the readout circuit is reduced from 1.66fF to 0.25fF (OS2) and the offset variation is reduced from 1.4fF to 0.2fF ($\delta 2$, from 0.1fF to 0.3fF). The nonlinearity of the readout circuit is also significantly reduced from 5.5% to 0.9% with an input signal range of 30fF. This is because the kickback charge injection is reduced. These measurement results demonstrate that the multi-nested clocks can significantly reduce the charge injection and charge injection variation introduced by the timing mismatch. Compared to [14] and [16] which were fabricated with the same IC process and reduced their input offset to sub-fF level by calibration method, this work consumes significantly less chip area. This is because this work does not require the calibration circuits used in [14] and [16] which consume a high proportion of their chip area. The reference [14] achieved a marginally better input offset (0.224fF), compared to this work, but it has more than doubled chip area (1.13mm^2). Furthermore, the calibration circuits used in the [14] and [16] do not take measures to reduce the nonlinearity while this work does. The final nonlinearity of this work (0.9%) is slight worse than that of [16] (0.8%). This is because the supply voltage used in this work (1.8V) is much lower than that in [16] (3.3V).

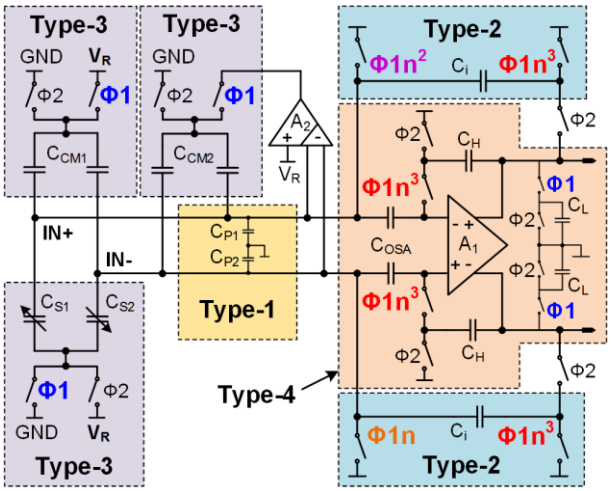


Fig. 12. Decomposition of the OSA readout circuit and the clock strategy employing multi-nested clocks.

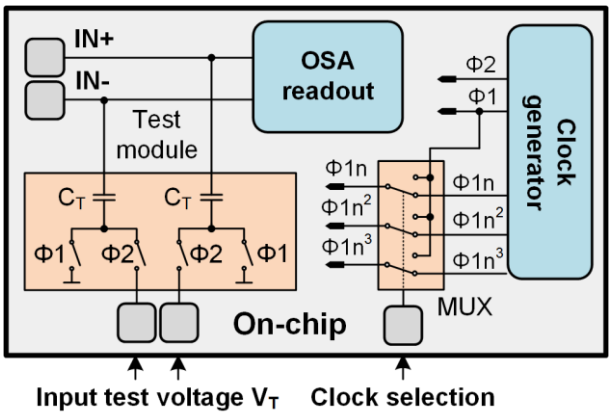


Fig. 13. Test configuration of the readout circuit.

V. Conclusions

In order to improve the precision of the readout circuit for capacitive sensor, a clock strategy using the multi-nested clocks is proposed and applied to a power-efficient OSA readout circuit in this paper. Compared to the OSA readout circuit employing a traditional clock scheme [7], the OSA readout circuit using the multi-nested clocks reduces the equivalent input offset from 1.66fF to 0.25fF and the offset variation from 1.4fF to 0.2fF. The nonlinearity measured by the output error of

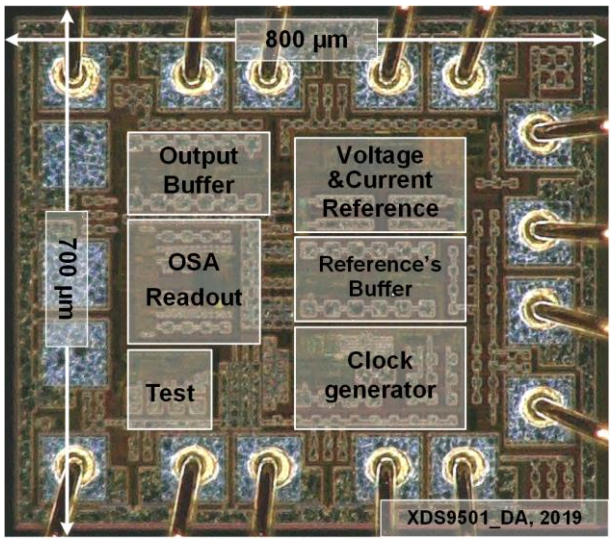


Fig. 14. Chip photograph of the readout circuit.

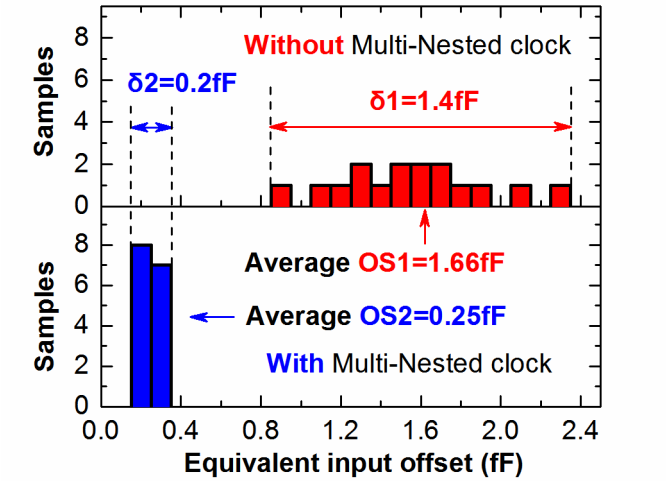


Fig. 15. Measurement results of the output signal of the readout circuit with and without multi-nested clocks, respectively.

TABLE I MAIN PARAMETERS SUMMARY AND COMPARISONS

	This work	[7]	[14]	[16]
Equ. input offset (fF)	**0.25**	**1.66**	**0.224**	**0.488**
Offset deviation (fF)	**0.2**	**1.4**	-	-
Non-linearity	**0.9%**	**5.5%**	-	**0.8%**
Chip area(mm^2)	**0.55**	**0.55**	**1.13***	**1.02***
IC Process (μm)	0.18	0.18	0.18	0.18
Full input range (fF)	±30	±30	-	±150
CVC sensitivity (mV/fF)	45	45	2	9.5
Supply voltage (V)	1.8	1.8	3.3	3.3
Power (μW)	451	450	980	220
Input noise (aF/√Hz)	1.9	1.9	0.088	1.275
Bandwidth (kHz)	10	10	0.4	0.4

*Data is estimated from the chip photograph excluding ADC which does not appear in this work in order to give a fair comparison.

the readout circuit with an input signal range of 30fF is reduced from 5.5% to 0.9%. Compared to another similar work [16] which reduced the offset of readout circuit to 0.488fF by the calibration method, this work achieves a better result with the offset of 0.25fF.

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